1014-68-1229 **Greta Pangborn*** (gpangborn@smcvt.edu), SMC Box 363, 1 Winooski Park, Colchester, VT 05439, and **Joanna Ellis-Monaghan**, **Paul Gutwin** and **Jamey Lewis**. *A Force-Directed Graph Drawing Approach for Computer Chip Layout.* Preliminary report.

We apply force-directed graph drawing to the industrial problem of physically laying out the components of a computer chip. A layout provides a geometrically constrained placement of the functional elements and their interconnections as specified by a netlist, a large data set encoding the abstract logical structure of a computer chip. Graphs naturally model the functional elements and interconnections of a netlist. However, the vertices represent rectangular chip elements with physical dimensions that must be placed on a chip without overlap. We have focused our attention on the floorplanning step (a rough mapping of where major subsections of the netlist should be placed), which is further complicated by widely varying block sizes and the fact that the blocks may be reshaped, having variable aspect ratios but not areas. We modify the traditional point mass spring-embedder graph drawing techniques to include gate viscosity variables that allow the rectangular vertices to pass through one another early in the process but repel one another later on to reduce gate overlap. We model the malleable blocks as rectangles responsive to penetration pressures from neighboring blocks. (Received September 28, 2005)