1096-94-926 **Kathryn A Haymaker*** (s-khaymak1@math.unl.edu), 203 Avery Hall, Department of Mathematics, University of Nebraska-Lincoln, Lincoln, NE 68588. *Structured LDPC codes for flash memory.*

The physical layout of flash memory imposes specific design constraints that affect how existing error-correcting codes are implemented in the memory. One such factor is that approximately half of stored bits have error probability b_1, while the remaining half have error probability b_2, with $b_1 < b_2$. A low-density parity-check (LDPC) code is the nullspace of a sparse matrix, and has a sparse bipartite graph representation that is amenable to efficient iterative message-passing decoding algorithms. In this work, we consider how to arrange codeword bits in the two sections of the memory so that the decoding probability of error goes to zero as the iteration number increases. Our analysis for binary codes leads to a design scheme for nonbinary codes that takes advantage of the differing bit-error probabilities. (Received September 11, 2013)